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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/254,939	03/17/99	MIURA H	500.36904X00

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EXAMINER	
MAI, A	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 08/28/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/254,939	Applicant(s) MIURA ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *09 November 2000* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination

1. The request filed on July 26, 2001 for a Continued Examination (RCE). An action on the RCE follows.

Claim Objections

2. Claim 16 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

As discloses in the specification (page 12), the providing the upper end portion of the trench with a curvature is done so by forming trench liner (a so-called "bird's beak" is formed between the contact portions. As a result, the radius of curvature in the proximity of the upper end of the silicon substrate 1 is promoted). Thus, claim 16 does not further limit claim 15 by claiming a same subject matter with a different term.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI).

Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) growing trench sidewall oxide in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (SiO_2) into the trench so oxidized;

(e) after burying the buried insulating film, oxidizing the semiconductor substrate;

(f) removing the buried insulating film formed on the oxidation prevention film (SiN);

(g) eliminating the oxidation prevention film formed on the semiconductor substrate; and

(h) after eliminating the oxidation prevention film, forming a gate oxide film. (See Figs. 2).

Regarding step (c) oxidizing the trench portion, Lee teaches that the trench sidewall oxide is grown. The term "grown" (oxide) is known in the art as thermally grown by subjecting silicon (substrate) to oxidizing ambient (wet or dry) under high temperature, hence oxidizing the trench portion.

Regarding the functional limitation of so as to provide a curvature of the upper end portion of the trench, the process of Lee includes oxidizing the semiconductor substrate having the buried insulating film formed therein, thus the oxidation of Lee is inherently result in the formation of the curvature at the upper corner of the trench. (see Fig. 7a).

Regarding the forming a gate oxide film in step (h), the device of Lee is a MOS device formed after the completion of the STI. The MOS device are well known in the art containing a gate oxide, thus the process of Lee includes forming a gate oxide film.

With respect to claims 18-20, the buried insulating film of Lee is oxide formed by CVD.

4. Claims 2, 3 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al in view of Kojiro (JP-01-107554).

As best understood by examiner, Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(c) forming trenches having a predetermined depth in the semiconductor substrate;

(d) growing trench sidewall oxide in the semiconductor substrate, exposed in the trenches;

(e) burying a buried insulating film (SiO_2) into the trench so oxidized;

(f) oxidizing the semiconductor substrate after burying the buried insulating film, so as to increase the curvature of the trenches corner;

(g) removing the buried insulating film formed on the oxidation prevention film (SiN);

(h) eliminating the oxidation prevention film formed on the semiconductor substrate; and

(i) after eliminating the oxidation prevention film, forming a gate oxide film. (See Figs. 2).

Thus, Lee is shown to teach all the features of the claim with the exception of forming the trenches using two steps etching and explicitly disclosing the formation of the trench sidewall oxide.

However, Kojiro '554 teaches forming a trench using two steps etch:

(1) forming shallow trenches having a radius curvature at the corners in a desired position of the circuit formation surface of a semiconductor substrate (1);

(2) forming trench having a predetermined depth to the shallow trenches.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches of Lee using two etching steps as taught by Kojiro to reduced leakage current.

Regarding step (c) oxidizing the trench portion, Lee teaches that the trench sidewall oxide is grown. The term "grown" (oxide) is known in the art as thermally grown by subjecting silicon (substrate) to oxidizing ambient (wet or dry) under high temperature, hence oxidizing the trench portion.

Regarding the functional limitation of so as to provide a curvature of the upper end portion of the trench, the process of Lee includes oxidizing the semiconductor substrate having

the buried insulating film formed therein, thus the oxidation of Lee is inherently result in the formation of the curvature at the upper corner of the trench. (see Fig. 7a).

With respect to claim 3, forming trenches by two steps of Kojiro includes an isotropic etching the exposed substrate follows by anisotropic etching of the earlier trench to a desired depth.

With respect to claims 21-23, the buried insulating film of Lee is oxide formed by CVD.

5. Claims 4 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta (U.S. Patent No. 5,679,599).

Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming a trench having a predetermined depth at a desired positions of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion (185) not covered by the oxidation prevention film (120);

(c) oxidizing trench portions formed in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (230) into the trench so oxidized;

(f) oxidizing the semiconductor substrate after the buried insulating film (230) formed on the oxidation prevention film (120) is removed, the upper end portions not covered by the oxidation prevention film being oxidized;

(g) removing the oxidation preventing film (120) formed on the circuit formation surface of the semiconductor substrate; and

(h) after the oxidizing the semiconductor substrate, forming a gate oxide film. (See Figs. 11-18).

Thus, Mehta is shown to teach all the features of the claim with the exception of explicitly disclosing the removal of the oxidation preventing film (120) and forming a gate oxide film.

However, the teaching of Mehta includes forming the isolation structure in an integrated circuit such as CMOS and memory devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the oxidation prevention film (120) and form the gate oxide on the semiconductor substrate of Mehta at the completion of the isolation structures since the process is well known and within the ability of a skill worker in the art prior to the forming the CMOS and the memory devices.

With respect to claims 24-26, the buried insulating film (230) of Mehta is oxide formed by CVD.

6. Claims 5, 6 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '599 in view of Kojiro '554.

Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (30);

(c) forming a trench (200) having a predetermined depth in the semiconductor substrate;

(d) oxidizing trench portions formed in the semiconductor substrate, exposed in the trench;

(e) burying a buried insulating film (230) into the trench so oxidized;

(f) removing the buried insulating film (230) formed on the oxidation prevention film;

(g) oxidizing the semiconductor substrate after the buried insulating film formed on the oxidation prevention film (230) is removed, so as to increase the curvature of the trench at the corners;

(h) removing the oxidation prevention film (120) formed on the circuit formation surface of the semiconductor substrate; and

(h) after the oxidizing the semiconductor substrate, forming a gate oxide film. (See Figs. 11-18).

Thus, Mehta is shown to teach all the features of the claim with the exception of forming the trenches using two steps etching and explicitly disclosing the removal of the oxidation preventing film (120) and forming a gate oxide film.

However, Kojiro '554 teaches forming a trench using two steps etch:

(1) forming shallow trenches having a radius curvature at the corners in a desired position of the circuit formation surface of a semiconductor substrate (1);

(2) forming trench having a predetermined depth to the shallow trenches.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches of Mehta using two etching steps as taught by Kojiro to reduced leakage current.

Further, the teaching of Mehta includes forming the isolation structure in an integrated circuit such as CMOS and memory devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the oxidation prevention film (120) and form the gate oxide on the semiconductor substrate of Mehta at the completion of the isolation structures since the process is well known and within the ability of a skill worker in the art prior to the forming the CMOS and the memory devices.

With respect to claim 6, forming trenches by two steps of Kojiro includes an isotropic etching the exposed substrate follows by anisotropic etching of the earlier trench to a desired depth.

With respect to claims 27-29, the buried insulating film of Mehta is oxide formed by CVD.

7. Claims 9 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.

Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming trench regions in the substrate from the circuit formation surface thereof;

(c) forming an oxide film on the trench regions formed in step (b);

(d) forming an insulating film (SiO_2) inside the oxide film (oxidized trench regions) so as to completely fill them;

(e) performing a second oxidation to selectively oxidize an opening side of the completely filled trench regions in the substrate; and

(f) after performing the second oxidation, forming a gate oxide film. (See Figs. 2).

Regarding the formation of the oxide film, Lee teaches that the trench sidewall oxide is grown. The term "grown" (oxide) is known in the art as thermally grown by subjecting silicon (substrate) to oxidizing ambient (wet or dry) under high temperature, hence performing a first oxidation.

Regarding the forming a gate oxide film in step (f), the device of Lee is a MOS device formed after the completion of the STI. The MOS device are well known in the art containing a gate oxide, thus the process of Lee includes forming a gate oxide film.

With respect to claims 30-32, the insulating film of Lee is oxide formed by CVD.

8. Claims 10-13 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.

Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) growing trench sidewall oxide in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (SiO_2) into the trench so oxidized;

(e) after burying the buried insulating film, providing the upper end portion of the trench with a curvature;

(f) removing the buried insulating film formed on the oxidation prevention film (SiN); and

(g) removing the oxidation prevention film formed on the circuit formation surface of the semiconductor substrate. (See Figs. 2).

Regarding oxidizing a trench portion, step (c), Lee teaches that the trench sidewall oxide is grown. The term "grown" (oxide) is known in the art as thermally grown by subjecting silicon (substrate) to oxidizing ambient (wet or dry) under high temperature, hence oxidizing the trench portion.

Regarding providing the upper end portion of the trench with a curvature, the process of Lee includes oxidizing the filled trench, the providing the upper end portion with a curvature.

With respect to claim 11, the thermally oxidizing the upper end portion has been discussed above.

With respect to claim 12, the providing the upper end portion with a curvature of Lee includes a well known bird's beak formation at the upper end portion of the trench. (see Otsu '861)

With respect to claim 13, the providing the curvature of Lee is formed such that an angle (θ) between the circuit formation surface of the semiconductor substrate and a side surface of the semiconductor substrate forming the trench is within a range of $90° < \theta > 180°$.

With respect to claims 33-35, the buried insulating film of Lee is oxide formed by CVD.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claim 10 above, and further in view of Mehta '599.

Lee is shown to teach all the features of the claim with the exception of providing the curvature is performed after removing the buried insulating film (SiO_2).

However, Mehta teaches the formation of the curvature can be performed after the removal of the insulating film (230) formed on the oxidation prevention film (120). (See Fig. 18).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to formed the curvature of Lee after the removal of the insulating film as taught by Mehta because less insulating film results more effective oxidation.

10. Claims 15-17 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.

Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) growing trench sidewall oxide in the semiconductor substrate, exposed in the trench, so as to provide the upper end portion of the trench with a curvature;

(d) burying a buried insulating film (SiO_2) into the trench so oxidized;

(e) removing the buried insulating film formed on the oxidation prevention film (SiN); and

(f) removing the oxidation prevention film formed on the circuit formation surface of the semiconductor substrate. (See Figs. 2).

Regarding oxidizing a trench portion, step (c), Lee teaches that the trench sidewall oxide is grown. The term "grown" (oxide) is known in the art as thermally grown by subjecting silicon (substrate) to oxidizing ambient (wet or dry) under high temperature, hence oxidizing the trench portion.

Regarding the functional limitation of so as to provide the upper end portion of the trench with a curvature, the trench sidewall of Lee is thermally grown, thus the upper end portion (corner) is inherently having a curvature.

With respect to claim 16, as best understood by examiner, the formation of the trench sidewall oxide also includes a formation of a bird's beak at the upper end portion of the trench, so as to provide the curvature.

With respect to claim 17, the oxidizing of Lee is thermal oxidation, so as to provide the curvature.

With respect to claims 36-38, the buried insulating film of Lee is oxide formed by CVD.

Response to Arguments

11. Applicant's arguments with respect to claims 1-6 and 9-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
August 23, 2001

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